Modeling of High Frequency Effects and Electric Field Induced Surface Charges for Power Electronic Systems

Jonathan Itokazu, PhD student
University of Wisconsin - Milwaukee
College of Engineering and Applied Sciences
Department of Electrical Engineering

Overview
The simultaneous higher switching frequency and higher device breakdown voltage capabilities of Wide Band Gap (WBG) power semiconductors will have a transformative impact on medium voltage distribution paradigms by enabling dynamic control of energy and power with significant reductions in through-put losses and equipment space-claim at voltage and power unachievable with present-day technology. The implementation of WBG power semiconductors in power electronic devices poses some significant challenges which arise from the high voltage edge rate (\(dv/dt\)) switching characteristics and high electric field in these WBG converters which results in significant Electromagnetic Interference (EMI) spectral content in the medium to high frequency (1-100MHz) range, and subsequently will change how power electronic converters are designed, packaged and applied. Additionally, the high electric field in WBG converters effects surface charges on conductive surfaces and heat sinks pose significant challenges for insulation design, achieving power density objectives and necessitates redefining creepage and clearance requirements. Current creepage and clearance requirements were derived from low voltage AC systems and if improperly applied can lead to reduced reliability of equipment, overly conservative designs, and potentially cancel out the benefits of WBG. The purpose of this research is to develop new modeling paradigms for high \(dv/dt\) high and high-field power electronic converters in order to enable a systematic evaluation of new design approaches, material applications and standards for testing.

Characterization of EMI

Spectral Considerations

Traditional insulated gate bipolar transistor (IGBT)-based systems have operational frequencies up to approximately 50 kHz and has content in the extended dynamics range which can be easily suppressed. Current techniques such as lumped element analysis works well and packaging impedances are managed by good layout and shielding techniques. WBG systems operate at higher frequencies has an extended dynamics range up to approximately 50 MHz. In this “Near-RF” range, lumped element analysis becomes inadequate and packaging impedances become critically important.

Modeling and Characterization of EMI

Movement of EMI producing content into the “Near-RF” domain changes the paradigm for EMI characterization, modeling and mitigation and wavelengths of EMI noise sources come into the range where the assumption that wavelengths are long with respect to circuit dimensions is no longer valid. As a result, capacitor and low turn-count inductors exhibit behavior dominated by parasitic effects and bus planes, cabling and high turn-count inductors become “electrically small” and begin to exhibit wave-like behavior.

Impacts of EMI

High electrical potentials on isolated heat sinks and high-frequency magnetic cores in the presence of high \(dv/dt\) induced displacement currents to equipment chassis introduce electrical-thermal-material coupling effects that can lead to the “EMI-induced” degradation of equipment.

An implementation of a MVDC interfacing power conversion systems implemented using a common WBG-based power electronic building block (PEBB) is shown above. The distribution of voltage from the points connected to the MVDC or MVAC bus cause the PEBB and lowest replaceable unit (LRU) heat sinks to have a build-up of surface charge. In the presence of high frequency switching power semiconductors, there is a propagation path for \(dv/dt\) across the modules’ direct bonded copper substrates (represented as capacitors from drain or source to heat sink in the blue areas). Multi-level structures divide the line-to-line MVDC or MVAC voltage between lower rated PEBBs. The uppermost connected devices, i.e. connected to the positive rail of the MVDC bus, must withstand the entire voltage with respect to ground (1\(V_{REF3}\)).

Within this system, there are parts where surface charges exist. These parts are not intended for electrical conduction and problems of slow surface flashover due to electrochemical, erosion and contamination mechanisms may occur. In the presence of surface contaminations and condensation high frequency \(dv/dt\) induced leakage currents may produce sufficient heating of the surface to remove the conducting film of local contamination. The sudden introduction of a high-resistance discontinuity in the conducting film may cause an electric spark to occur at the site of the discontinuity. The sparks, which occur at each break in the conducting layer, can cause degradation of the insulator surfaces, which is known as breakdown by tracking. These surface charge effects are in addition to the potential for dielectric breakdown across insulating surfaces. The red areas depicted in the system represent the means by which heat sinks are isolated from the chassis/ground and are subject to the same effects mentioned above. Optimal solutions which attempt to maximize power density by shaping electric field distribution through materials and geometries for the magnetic components have been studied, but in practice, this problem is addressed by increasing spacing between cells, which significantly reduces system power density and subsequently impose creepage and clearance requirements which negate any of the advantages presented by WBG power semiconductors.

Objective

Increasing the MVDC level should reduce current stresses on the converter cells in the MMLC however, the need for dielectric stand-off distances between the individual cells in the MMLC results in a degradation in power density as the voltage level of the system increases. The effect of this can be seen on the right (a). If we are able to reduce these distances, we would be able to achieve power densities greater than a factor of two times the power densities achieved with current distances (b). In order to achieve this, the expected voltage stress across the insulation and heat sinks in the ungrounded system needs to be determined, as it directly influences creepage.

Methodology

A silicon carbide MOSFET based inverter operating at a switching frequency of 100 kHz in a half-bridge configuration was used as a test case to develop the methodology and metrology for an accurate measurement of the baseplate current through the module, heatsink and chassis in a ground plane. The results of this test indicated that the internal module to heat sink capacitances and the heat sink to ground impedance established the common mode (CM) voltages produced for frequencies greater than 100 kHz.

Current methods in modeling which employ lumped element analysis do not provide accurate modeling of the device under test (DUT), thus he methodology proposed defines the CM and DM current and voltages with respect to an arbitrary reference point \(p\) as

\[
i_{CM} = \sum_{n=1}^{N} i_{n}
\]

\[
i_{EM} \triangleq \frac{1}{N} (i_{n+1} - i_{n})
\]

and there are \(N \times 1\) DM voltage definitions and one CM current which can be considered to be a \(N \times N\) linear transform of the mixed mode (MM) quantities to decomposed DM and CM quantities expressed as

\[
i_{CM} \triangleq (T_{D} i_{c})
\]

\[
i_{DM} \triangleq (T_{C} i_{c})
\]

Where \(i_{c}\) and \(v_{c}\) are the vector of the MM line currents and voltages respectively, and \(T_{D}\) and \(T_{C}\) are the vectors of DM and CM currents respectively. In expanded form,

\[
[T_{D}\ T_{C}] \begin{bmatrix}
i_{c}(n+1) \\
i_{c}(n) \\
i_{c}(n-1) \\
\vdots \\
i_{c}(1)
\end{bmatrix} = \begin{bmatrix}
\frac{1}{N} & -\frac{1}{N} & \frac{0}{N} & \frac{0}{N} & \cdots & \frac{0}{N} \\
\frac{0}{N} & \frac{1}{N} & -\frac{1}{N} & \frac{0}{N} & \cdots & \frac{0}{N} \\
\frac{0}{N} & \frac{0}{N} & \frac{1}{N} & -\frac{1}{N} & \cdots & \frac{0}{N} \\
\frac{\cdots}{\cdots} & \frac{\cdots}{\cdots} & \frac{\cdots}{\cdots} & \frac{\cdots}{\cdots} & \cdots & \frac{\cdots}{\cdots} \\
\frac{1}{N} & \frac{\cdots}{\cdots} & \frac{\cdots}{\cdots} & \frac{\cdots}{\cdots} & \cdots & \frac{1}{N}
\end{bmatrix} \begin{bmatrix}
i_{c}(n+1) \\
i_{c}(n) \\
i_{c}(n-1) \\
\vdots \\
i_{c}(1)
\end{bmatrix}
\]

With these definitions, we are able to derive a CM equivalent model of the DUT as shown on the right. With this equivalent model, we can begin to accurately model the voltage stresses induced from switching across various points throughout the system which is a first step in understanding and redefining the creepage and clearance requirements.

Future work will be on formalizing this methodology and implementing it across various power electronic systems with the intent to characterize the EMI and the hope to implement mitigation techniques which will increase current power density benchmarks.